

FIG. 1 is a block diagram of a transmitter circuit 100. The transmitter circuit 100 includes a data input 102, a clock input 104, a carrier signal input 106, a register 108, a first AND gate 110, a second AND gate 116, a first differential pair 112, a second differential pair 114, a third differential pair 118, a fourth differential pair 120, and an antenna 124. The data input 102 is connected to the D input of the register 108. The clock input 104 is connected to the clock input of the register 108. The carrier signal input 106 is connected to the input of the second AND gate 116. The output of the register 108 is connected to the input of the first AND gate 110. The output of the first AND gate 110 is connected to the gates of the first and second differential pairs 112 and 114. The output of the second AND gate 116 is connected to the gates of the third and fourth differential pairs 118 and 120. The drains of the first and second differential pairs 112 and 114 are connected to a common node, which is connected to the antenna 124. The drains of the third and fourth differential pairs 118 and 120 are connected to a common node, which is connected to the antenna 124. The sources of the first and second differential pairs 112 and 114 are connected to a common node, which is connected to ground. The sources of the third and fourth differential pairs 118 and 120 are connected to a common node, which is connected to ground. The antenna 124 is connected to a Tx terminal.

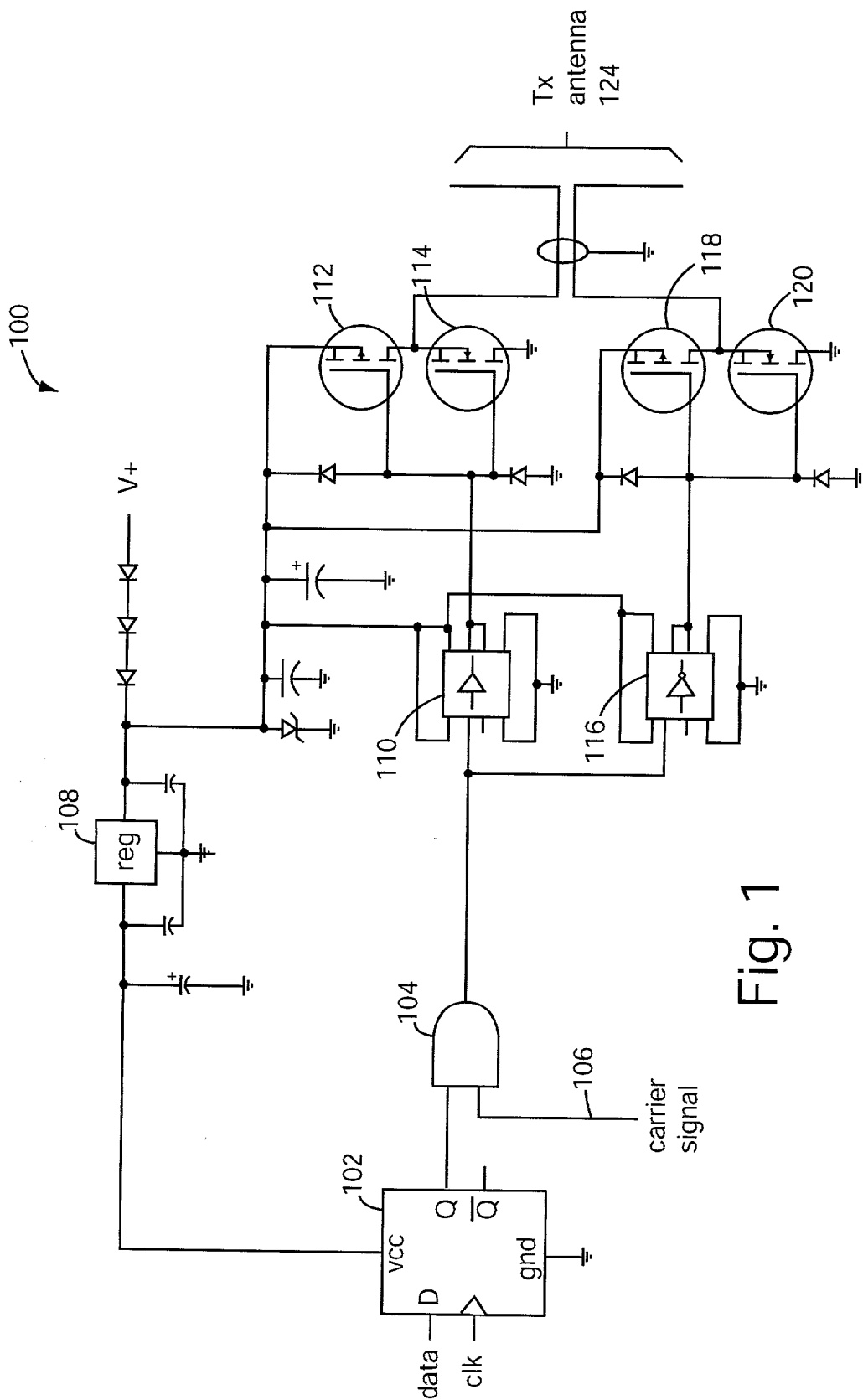


Fig. 1

200

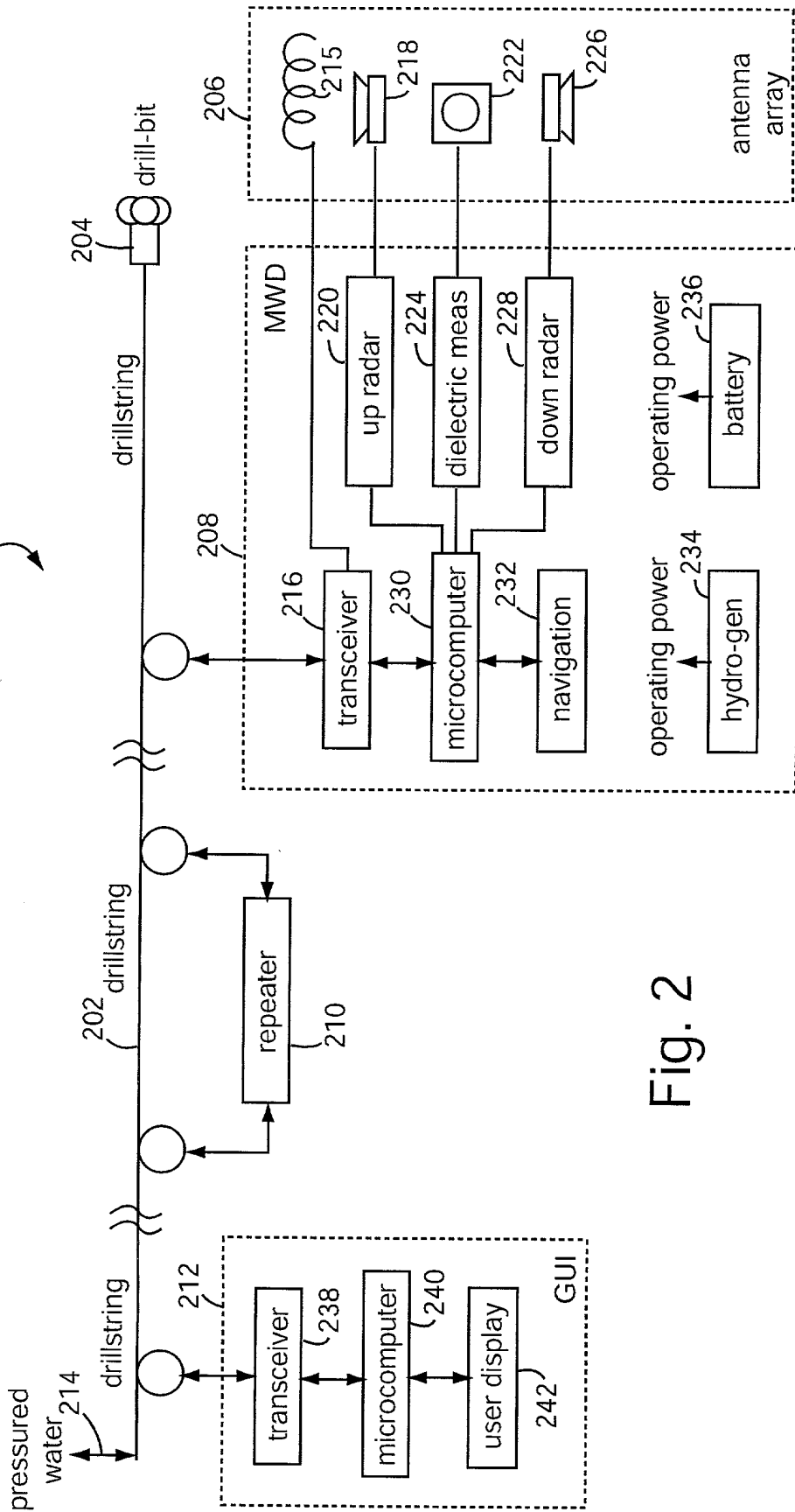


Fig. 2